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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/558,542	04/26/2000	Sri Ram Gorti	105178	9596

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EXAMINER	
NAHAR, QAMRUN	
ART UNIT	**PAPER NUMBER**
2124	10

DATE MAILED: 01/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/558,542	Applicant(s) GORTI ET AL.	
	Examiner Qamrun Nahar	Art Unit 2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-13 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-13 and 15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to the RCE filed on 11/12/03.

2. The rejection under 35 U.S.C. 102(b) as being anticipated by Benson (U.S. 5,301,325) to claims 1-20 is moot in view of the new ground(s) of rejection.

3. Claims 4 and 14 have been cancelled.

4. Claims 1 and 11 have been amended.

5. Claims 1-3, 5-13 and 15-20 are pending.

6. The objections to claims 5 and 15 are pending.

7. Claims 1-3, 5-13 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Benson (U.S. 5,301,325) in view of Sato (U.S. 5,261,062).

Response to Amendment

Claim Objections

8. Claims 5 and 15 are objected to because of the following informalities: these claims depend on cancelled claims. Claims 5 and 15 are interpreted as depending on claims 3 and 13, respectively.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-3, 5-13 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Benson (U.S. 5,301,325) in view of Sato (U.S. 5,261,062).

Per Claim 1 (Amended):

Benson teaches a code translation device that translates a source code of a source processor into a target code of a target processor ("In accordance with one embodiment of the invention, a code translator is constructed in a manner similar to a compiler, and may indeed be implemented as part of a compiler. The code translator accepts as an input the assembly code or source code which is to be translated, in a manner similar to the front end of any compiler. The input code is parsed to determine its content, with the basic building blocks of the code identified (separated) and converted into an intermediate language. The intermediate language version of the code is stored in a data structure referred to as a flow graph. The flow graph is referenced by flow analyzer techniques and optimization routines, before generating object code for the target machine. This translator is particularly adapted for translating VAX assembly language into an advanced RISC architecture." in column 4, lines 3-18); a memory ("Fig. 2 is an electrical diagram of a host computer for executing the code translator program of Fig. 1" in column 7, lines 44-45 and Fig. 2, item 15, "MEMORY"); a controller, the controller dividing the source code into code blocks based on one or more instructions of the source code that either includes a branch, a loop return or an entry point for a branch or loop return ("The code translator accepts as an input the assembly code or source code which is to be translated, in a manner similar to the front end of any compiler. The input code is parsed to determine its content, with the basic

building blocks of the code identified (separated) and converted into an intermediate language. The intermediate language version of the code is stored in a data structure referred to as a flow graph. The flow graph is referenced by flow analyzer techniques and optimization routines, before generating object code for the target machine. ... Another feature of interest in converting code from one architecture to another is that of register usage. ... In code generated by the compiler for register saves for an advanced 64-bit RISC architecture, only the low 32-bits of the 64-bit register can be put on the stack ... Accordingly, in one embodiment of the invention, the compiler tracks register usage to determine which registers are destroyed by a routine, and generate routine prologue and epilogue code which performs 64-bit register saves." in column 4, lines 3-18 and lines 44-61; column 4, lines 67-68 to column 5, lines 1-18; and column 10, lines 20-30). Benson does not explicitly teach that the controller dividing the source code into code blocks based on a target processor register capability, wherein the controller identifies source register types as data registers or address registers of the source processor and corresponding target registers of the target processor that correspond to each of the source register types, the controller selecting one or more selected source register types and one or more maximum numbers of corresponding target registers that correspond to the selected source register types as the target register capability.

Sato teaches that the controller dividing the source code into code blocks based on a target processor register capability, wherein the controller identifies source register types as data registers or address registers of the source processor and corresponding target registers of the target processor that correspond to each of the source register types, the controller selecting one or more selected source register types and one or more maximum numbers of corresponding

target registers that correspond to the selected source register types as the target register capability ("In accordance with the present invention, there is disclosed a register allocation method adaptive for a pipelining system in which after allocation of registers to be used for a plurality of instructions included in a program, relocation of said plurality of instructions can be performed, and the plurality of instructions can be executed in parallel to perform arithmetic operation processing, wherein the registers are allocated to the plurality of instructions to be executed on a parallel basis in such a manner that respective ones of the instructions are provided with associated ones of the registers, if the number of interferences, which indicates the number of registers to be simultaneously used by the plurality of instructions at a predetermined timing during the arithmetic operation processing, does not exceed the total number of the registers. In accordance with one aspect of the present invention, the number of interferences, which indicates the number of registers to be simultaneously used by the plurality of instructions at a predetermined timing during the arithmetic operation processing, is retrieved, and as a result, if it is equal to or less than the total number of said registers, the registers are allocated to the instructions to be executed on a parallel basis in such a manner that each individual one of the instructions is provided with the associated one of the registers ... as shown in FIG. 1A, three real registers r0, r1 and r2 are allocated to the virtual registers." in column 2, lines 55-68 to column 3, lines 1-16; and column 3, lines 58-61; "virtual registers" are interpreted as source registers and "real registers" are interpreted as target registers; Fig. 7 shows an example of source register types as data registers or address registers).

It would have been obvious to one having ordinary skill in the computer art at the time of the invention was made to modify the device disclosed by Benson to include that the controller

dividing the source code into code blocks based on a target processor register capability, wherein the controller identifies source register types as data registers or address registers of the source processor and corresponding target registers of the target processor that correspond to each of the source register types, the controller selecting one or more selected source register types and one or more maximum numbers of corresponding target registers that correspond to the selected source register types as the target register capability using the teaching of Sato. The modification would be obvious because one of ordinary skill in the art would be motivated to increase processing speed, where the number of registers are limited (Sato, column 1, lines 39-45).

Per Claim 2:

The rejection of claim 1 is incorporated, and Benson further teaches a branch detector, the branch detector identifying one or more instructions of the source code that either includes a branch, a loop return or an entry point for a branch or loop return (column 4, lines 44-61 and column 10, lines 20-30).

Per Claim 3:

The rejection of claim 2 is incorporated, and Benson further teaches wherein the controller generates one or more source code blocks based on the identified instructions, each of the source code blocks beginning immediately after an identified instruction and includes all consecutive instructions following the identified instruction up to an instruction immediately before a next identified instruction (column 10, lines 20-36 and lines 44-66).

Per Claim 5:

The rejection of claim 3 is incorporated, and Sato further teaches further comprising a register detector, the register detector detecting a number of source registers that are used and/or updated in one or more instructions of each of the source code blocks (column 4, lines 17-27).

Per Claim 6:

The rejection of claim 5 is incorporated, and Sato further teaches wherein the controller generates one or more translated code blocks for each of the source code blocks based on a number of selected source registers detected by the register detector and the maximum numbers of corresponding target registers (column 4, lines 48-68 to column 5, lines 1-9).

Per Claim 7:

The rejection of claim 6 is incorporated, and Benson further teaches a stub generator, the stub generator generating a head stub and a tail stub for each of the translated code blocks (column 5, lines 14-18).

Per Claim 8:

The rejection of claim 7 is incorporated, and Benson further teaches wherein a head stub associated with a translated code block initializes one or more target registers used by the associated translated code block, the target registers being initialized by retrieving register values from a source register map that stores values of the source registers during execution of the

translated code blocks (column 5, lines 18-43; column 6, lines 57-68 to column 7, lines 1-7; and column 7, lines 19-30).

Per Claim 9:

The rejection of claim 7 is incorporated, and Benson further teaches wherein a tail stub associated with a translated code block saves values of one or more target registers used by the associated translated code block in a source register map after execution of the translated code block (column 5, lines 18-40 and lines 45-47; column 6, lines 57-68 to column 7, lines 1-7; and column 7, lines 19-30).

Per Claim 10:

The rejection of claim 9 is incorporated, and Sato further teaches wherein the source register map includes storage space for one or more values for each source register accounting for instruction execution delays, the tail stub saves values of the target registers in one or more appropriate locations in the source register map to account for the instruction execution delays (column 4, lines 63-68 to column 5, lines 1-2).

Per Claim 11 (Amended):

This is a method version of the claimed device discussed above, claim 1, wherein all claim limitations also have been addressed and/or covered in cited areas as set forth above, including "identifying a target processor register capability" (Sato, column 2, lines 55-68 to column 3, lines 1-16). Thus, accordingly, this claim is also obvious.

Per Claims 12-13 & 15-20:

These are method versions of the claimed device discussed above (claims 2-3 & 5-10, respectively), wherein all claim limitations also have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also obvious.

Response to Arguments

11. Applicant's arguments with respect to claims 1-3, 5-13 and 15-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. Any inquiry concerning this communication from the examiner should be directed to Qamrun Nahar whose telephone number is (703) 305-7699. The examiner can normally be reached on Mondays through Thursdays from 9:00 AM to 6:30 PM. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki, can be reached on (703) 305-9662. The fax phone number for the organization where this application or processing is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

QN
January 21, 2004

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100